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(71) Applicant *(for all designated States except US)*: NORTH CAROLINA STATE UNIVERSITY [US/US]; 1 Holladay Hall, Campus Box 7003, Raleigh, NC 27695–7003 (US).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: LINTHICUM, Kevin, J. [US/US]; 474 Crosslink Drive, Angier, NC 27501 (US). GEHRKE, Thomas [DE/US]; 116B Bim Street, Carrboro, NC 27510 (US). THOMSOM, Darren, B. [US/US]; 425 W. Cornwall Road, Cary, NC 27511 (US). CARLSON, Eric, P. [US/US]; 1208 Southern Oaks Drive, Raleigh, NC 27603 (US). RAJAGOPAL, Pradeep [IN/US]; Apartment 102, 2502 Avent Ferry Road, Raleigh, NC 27606 (US). DAVIS, Robert, F. [US/US]; 5705 Calton Drive, Raleigh, NC 27612 (US).

(74) Agents: BIGEL, Mitchell, S. et al.; Myers, Bigel, Sibley, & Sajovec, P.A., P.O. Box 37428, Raleigh, NC 27627 (US).

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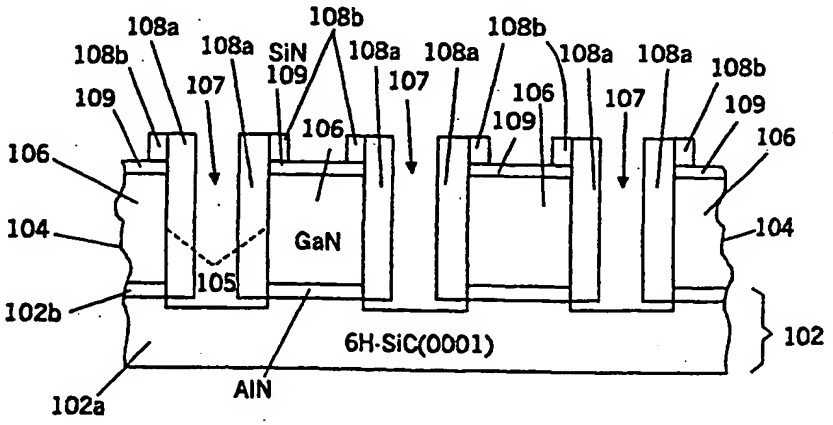

(57) Abstract

An underlying gallium nitride layer (104) on a silicon carbide substrate (102) patterned with a mask (109) that includes an array of openings therein, and is etched through the array of openings to define posts (106) in the underlying gallium nitride layer and trenches (107) therebetween. The posts each include a sidewall (105) and a top having the mask thereon. The sidewalls of the posts are laterally grown into the trenches to thereby form a gallium nitride semiconductor layer (108a). During this lateral growth, the mask prevents nucleation and vertical growth from the tops of the posts. Accordingly, growth proceeds laterally into the trenches, suspended from the sidewalls of the posts. The sidewalls of the posts may be laterally grown into the trenches until the laterally grown sidewalls coalesce in the trenches to thereby form a gallium nitride semiconductor layer. The lateral growth from the sidewalls of the posts may be continued so that the gallium nitride layer grows vertically through the openings in the mask and laterally overgrows onto the mask on the tops of the posts, to thereby form a gallium nitride semiconductor layer (108b). The lateral overgrowth can be continued until the grown sidewalls coalesce on the mask to thereby form a continuous gallium nitride semiconductor layer. Microelectronic devices (110) may be formed in the continuous gallium nitride semiconductor layer.

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FABRICATION OF GALLIUM NITRIDE LAYERS BY LATERAL GROWTH

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Field of the Invention

This invention relates to microelectronic devices and fabrication methods, and more particularly to gallium nitride semiconductor devices and fabrication methods therefor.

Background of the Invention

Gallium nitride is being widely investigated for microelectronic devices including but not limited to transistors, field emitters and optoelectronic devices. It will be understood that, as used herein, gallium nitride also includes alloys of gallium nitride such as aluminum gallium nitride, indium gallium nitride and aluminum indium gallium nitride.

A major problem in fabricating gallium nitride-based microelectronic devices is the fabrication of gallium nitride semiconductor layers having low defect densities. It is known that one contributor to defect density is the substrate on which the gallium nitride layer is grown. Accordingly, although gallium nitride layers have been grown on sapphire substrates, it is known to reduce defect density by growing gallium nitride layers on aluminum nitride buffer layers which are themselves formed on silicon

carbide substrates. Notwithstanding these advances, continued reduction in defect density is desirable.

It is also known to fabricate gallium nitride structures through openings in a mask. For example, in fabricating field emitter arrays, it is known to selectively grow gallium nitride on stripe or circular patterned substrates. See, for example, the publications by Nam et al. entitled *"Selective Growth of GaN and $Al_{0.2}Ga_{0.8}N$ on GaN/AlN/6H-SiC(0001) Multilayer Substrates Via Organometallic Vapor Phase Epitaxy"*, Proceedings of the Materials Research Society, December 1996, and *"Growth of GaN and $Al_{0.2}Ga_{0.8}N$ on Patterened Substrates via Organometallic Vapor Phase Epitaxy"*, Japanese Journal of Applied Physics., Vol. 36, Part 2, No. 5A, May 1997, pp. L532-L535. As disclosed in these publications, undesired ridge growth or lateral overgrowth may occur under certain conditions.

Summary of the Invention

It is therefore an object of the present invention to provide improved methods of fabricating gallium nitride semiconductor layers, and improved gallium nitride layers so fabricated.

It is another object of the invention to provide methods of fabricating gallium nitride semiconductor layers that can have low defect densities, and gallium nitride semiconductor layers so fabricated.

These and other objects are provided, according to the present invention, by masking an underlying gallium nitride layer on a silicon carbide substrate with a mask that includes an array of openings therein and etching the underlying gallium nitride layer through the array of openings to define a plurality of posts in the underlying gallium nitride layer and a plurality of trenches therebetween. The posts each include a sidewall and a top having the mask thereon. The sidewalls of the posts are laterally grown into the trenches to thereby form a gallium nitride semiconductor layer. During this lateral growth, the mask prevents nucleation and vertical growth from the tops of the posts. Accordingly, growth proceeds laterally into the trenches, suspended from the sidewalls of the posts. This form of growth is referred to herein as pendeoepitaxy from the Latin "to hang" or "to be suspended". Microelectronic devices may be formed in the gallium nitride semiconductor layer.

According to another aspect of the invention, the sidewalls of the posts are laterally grown into the trenches until the laterally grown sidewalls coalesce in the trenches to thereby form a gallium nitride semiconductor layer. The lateral growth from the sidewalls of the posts may be continued so that the gallium nitride layer grows vertically through the openings in the mask and laterally overgrows onto the mask on the tops of the posts, to thereby form a gallium nitride semiconductor layer. The lateral overgrowth can be continued until the grown sidewalls coalesce on the mask to thereby form a continuous gallium nitride semiconductor layer. Microelectronic devices may be formed in the continuous gallium nitride semiconductor layer.

It has been found, according to the present invention, that dislocation defects do not significantly propagate laterally from the sidewalls of the posts, so that the laterally grown sidewalls of the posts are relatively defect-free. Moreover, during growth, it has been found that significant vertical growth on the top of the posts is prevented by the mask so that relatively defect-free lateral growth occurs from the sidewalls onto the mask. Significant nucleation on the top of the posts also preferably is prevented. The overgrown gallium nitride semiconductor layer is therefore relatively defect-free.

Accordingly, the mask functions as a capping layer on the posts that forces the selective homoepitaxial growth of gallium nitride to occur only on the sidewalls. Defects associated with heteroepitaxial growth of the gallium nitride seed layer are pinned under the mask. By using a combination of growth from sidewalls and lateral overgrowth, a complete coalesced layer of relatively defect-free gallium nitride may be fabricated over the entire surface of a wafer in one regrowth step.

The pendeoepitaxial gallium nitride semiconductor layer may be laterally grown using metalorganic vapor phase epitaxy (MOVPE). For example, the lateral gallium nitride layer may be laterally grown using triethylgallium (TEG) and ammonia (NH_3) precursors at about 1000-1100°C and about 45 Torr. Preferably, TEG at about 13-39μmol/min and NH_3 at about 1500 sccm are used in combination with about 3000 sccm H_2 diluent. Most preferably, TEG at about 26μmol/min, NH_3 at about 1500 sccm and H_2 at about 3000 sccm at a temperature of about 1100°C and about 45 Torr are used. The underlying gallium nitride layer preferably is formed on a substrate such as 6H-SiC(0001), which itself includes a buffer layer such as

aluminum nitride thereon. Other buffer layers such as gallium nitride may be used. Multiple substrate layers and buffer layers also may be used.

The underlying gallium nitride layer including the sidewall may be formed by forming trenches in the underlying gallium nitride layer, such that the trenches define the sidewalls. Alternatively, the sidewalls may be formed by forming masked posts on the underlying gallium nitride layer, the masked posts including the sidewalls and defining the trenches. A series of alternating trenches and masked posts is preferably formed to form a plurality of sidewalls. The posts are formed such that the top surface and not the sidewalls are masked. As described above, trenches and/or posts may be formed by masking and selective etching. Alternatively, selective epitaxial growth, combinations of etching and growth, or other techniques may be used. The mask may be formed on the post tops after formation of the posts. The trenches may extend into the buffer layer and/or into the substrate so that the trench floors are in the buffer layer and preferably are in the silicon carbide substrate.

The sidewalls of the posts in the underlying gallium nitride layer are laterally grown into the trenches, to thereby form a lateral gallium nitride layer of lower defect density than that of the underlying gallium nitride layer. Some vertical growth may also occur in the trenches, although vertical growth from the post tops is reduced and preferably suppressed by the mask thereon. The laterally grown gallium nitride layer is vertically grown through the openings in the mask while propagating the lower defect density. As the height of the vertical growth extends through the openings in the mask, lateral growth over the mask occurs while propagating the lower defect density to thereby form an overgrown lateral gallium nitride layer on the mask.

Gallium nitride semiconductor structures according to the invention comprise a silicon carbide substrate and a plurality of gallium nitride posts on the silicon carbide substrate. The posts each include a sidewall and a top and define a plurality of trenches therebetween. A capping layer is provided on the tops of the posts. A lateral gallium nitride layer extends laterally from the sidewalls of the posts into the trenches. The lateral gallium nitride layer may also be referred to as a pendeoepitaxial gallium nitride layer. The lateral gallium nitride layer may be a continuous lateral gallium nitride layer that extends between adjacent sidewalls across the trenches therebetween.

The lateral gallium nitride layer may also extend vertically through the array of openings. An overgrown lateral gallium nitride layer may also be provided that extends laterally onto the capping layer. The overgrown lateral gallium nitride layer may be a continuous overgrown lateral gallium nitride layer that extends between the adjacent sidewalls across the capping layer therebetween.

A plurality of microelectronic devices may be provided in the lateral gallium nitride layer and/or in the overgrown lateral gallium nitride layer. A buffer layer may be included between the silicon carbide substrate and the plurality of posts. The trenches may extend into the silicon carbide substrate, into the buffer layer or through the buffer layer and into the silicon carbide substrate. The gallium nitride posts may be of a defect density, and the lateral gallium nitride layer and the overgrown lateral gallium nitride layer are of lower defect density than the defect density. Accordingly, low defect density gallium nitride semiconductor layers may be produced, to thereby allow the production of high performance microelectronic devices.

Brief Description of the Drawings

Figures 1-6 are cross-sectional views of gallium nitride semiconductor structures during intermediate fabrication steps according to the present invention.

Figures 7 and 8 are cross-sectional views of other embodiments of gallium nitride semiconductor structures according to the present invention.

Detailed Description of Preferred Embodiments

The present invention now will be described more fully hereinafter with reference to the accompanying drawings, in which preferred embodiments of the invention are shown. This invention may, however, be embodied in many different forms and should not be construed as limited to the embodiments set forth herein; rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art. In the drawings, the thickness of layers and regions are exaggerated for clarity. Like numbers refer to like elements throughout. It will be understood that when an element such as a layer, region or substrate is referred to as being "on" or "onto" another element, it can be directly on the other element or intervening elements may

also be present. Moreover, each embodiment described and illustrated herein includes its complementary conductivity type embodiment as well.

Referring now to Figures 1-6, methods of fabricating gallium nitride semiconductor structures according to the present invention will now be described. As shown in Figure 1, an underlying gallium nitride layer **104** is grown on a substrate **102**. The substrate **102** may include a 6H-SiC(0001) substrate **102a** and an aluminum nitride or other buffer layer **102b**. The crystallographic designation conventions used herein are well known to those having skill in the art, and need not be described further. The underlying gallium nitride layer **104** may be between 0.5 and 2.0μm thick, and may be grown at 1000°C on a high temperature (1100°C) aluminum nitride buffer layer **102b** that was deposited on the 6H-SiC substrate **102a** in a cold wall vertical and inductively heated metalorganic vapor phase epitaxy system using triethylgallium at 26μmol/min, ammonia at 1500 sccm and 3000 sccm hydrogen diluent. Additional details of this growth technique may be found in a publication by T.W. Weeks et al. entitled *"GaN Thin Films Deposited Via Organometallic Vapor Phase Epitaxy on (6H)-SiC(0001) Using High-Temperature Monocrystalline AlN Buffer Layers"*, Applied Physics Letters, Vol. 67, No. 3, July 17, 1995, pp. 401-403, the disclosure of which is hereby incorporated herein by reference. Other silicon carbide substrates, with or without buffer layers, may be used.

Continuing with the description of Figure 1, a mask such as a silicon nitride (SiN) mask **109** is included on the underlying gallium nitride layer **104**. The mask **109** may have a thickness of about 1000Å and may be formed on the underlying gallium nitride layer **104** using low pressure chemical vapor deposition (CVD) at 410°C. The mask **109** is patterned to provide an array of openings therein, using conventional photolithography techniques.

As shown in Figure 1, the underlying gallium nitride layer is etched through the array of openings to define a plurality of posts **106** in the underlying gallium nitride layer **104** and a plurality of trenches **107** therebetween. The posts each include a sidewall **105** and a top having the mask **109** thereon. It will also be understood that although the posts **106** and trenches **107** are preferably formed by masking and etching as described above, the posts may also be formed by selectively growing the posts from an underlying gallium nitride layer and then forming a capping layer on

the tops of the posts. Combinations of selective growth and selective etching may also be used.

Still referring to Figure 1, the underlying gallium nitride layer **104** includes a plurality of sidewalls **105** therein. It will be understood by those having skill in the art that the sidewalls **105** may be thought of as being defined by the plurality of spaced apart posts **106**, that also may be referred to as "mesas", "pedestals" or "columns". The sidewalls **105** may also be thought of as being defined by the plurality of trenches **107**, also referred to as "wells", in the underlying gallium nitride layer **104**. The sidewalls **105** may also be thought of as being defined by a series of alternating trenches **107** and posts **106**. As described above, the posts **106** and the trenches **107** that define the sidewalls **105** may be fabricated by selective etching and/or selective epitaxial growth and/or other conventional techniques. Moreover, it will also be understood that the sidewalls need not be orthogonal to the substrate **102**, but rather may be oblique thereto.

It will also be understood that although the sidewalls **105** are shown in cross-section in Figure 1, the posts **106** and trenches **107** may define elongated regions that are straight, V-shaped or have other shapes. As shown in Figure 1, the trenches **107** may extend into the buffer layer **102b** and into the substrate **102a**, so that subsequent gallium nitride growth occurs preferentially on the sidewalls **105** rather than on the trench floors. In other embodiments, the trenches may not extend into the substrate **102a**, and also may not extend into the buffer layer **102b**, depending, for example, on the trench geometry and the lateral versus vertical growth rates of the gallium nitride.

Referring now to Figure 2, the sidewalls **105** of the underlying gallium nitride layer **104** are laterally grown to form a lateral gallium nitride layer **108a** in the trenches **107**. Lateral growth of gallium nitride may be obtained at 1000-1100°C and 45 Torr. The precursors TEG at 13-39μmol/min and NH_3 at 1500 sccm may be used in combination with a 3000 sccm H_2 diluent. If gallium nitride alloys are formed, additional conventional precursors of aluminum or indium, for example, may also be used. As used herein, the term "lateral" means a direction that is parallel to the faces of the substrate **102**. It will also be understood that some vertical growth of the lateral gallium nitride **108a** may also take place during the lateral growth from the sidewalls **105**. As used herein, the term "vertical" denotes a directional parallel to the sidewalls

105. However, it will be understood that growth and/or nucleation on the top of the posts 106 is reduced and is preferably eliminated by the mask 109.

Referring now to Figure 3, continued growth of the lateral gallium nitride layer 108a causes vertical growth of the lateral gallium nitride layer 108a through the array of openings. Conditions for vertical growth may be maintained as was described in connection with Figure 2. As also shown in Figure 3, continued vertical growth into trenches 107 may take place at the bottom of the trenches.

Referring now to Figure 4, continued growth of the lateral gallium nitride layer 108a causes lateral overgrowth onto the mask 109. to form an overgrown lateral gallium nitride layer 108b. Growth conditions for overgrowth may be maintained as was described in connection with Figure 2.

Referring now to Figure 5, growth is allowed to continue until the lateral growth fronts coalesce in the trenches 107 at the interfaces 108c, to form a continuous lateral gallium nitride semiconductor layer 108a in the trenches.

Still referring to Figure 5, growth is also allowed to continue until the lateral overgrowth fronts coalesce over the mask 109 at the interfaces 108d, to form a continuous overgrown lateral gallium nitride semiconductor layer 108b. The total growth time may be approximately 60 minutes. A single continuous growth step may be used. As shown in Figure 6, microelectronic devices 110 may then be formed in the lateral gallium nitride semiconductor layer 108a. Microelectronic devices also may be formed in the overgrown lateral gallium nitride layer 108b.

Accordingly, in Figure 6, gallium nitride semiconductor structures 100 according to the present invention are illustrated. The gallium nitride structures 100 include the substrate 102. The substrate preferably includes the 6H-SiC(0001) substrate 102a and the aluminum nitride buffer layer 102b on the silicon carbide substrate 102a. The aluminum nitride buffer layer 102b may be 0.1μm thick.

The fabrication of the substrate 102 is well known to those having skill in the art and need not be described further. Fabrication of silicon carbide substrates are described, for example, in U.S. Patents 4,865,685 to Palmour; Re 34,861 to Davis et al.; 4,912,064 to Kong et al. and 4,946,547 to Palmour et al., the disclosures of which are hereby incorporated herein by reference.

The underlying gallium nitride layer 104 is also included on the buffer layer 102b opposite the substrate 102a. The underlying gallium nitride layer 104 may be

between about 0.5 and 2.0μm thick, and may be formed using metalorganic vapor phase epitaxy (MOVPE). The underlying gallium nitride layer generally has an undesired relatively high defect density. For example, dislocation densities of between about 10^8 and $10^{10}cm^{-2}$ may be present in the underlying gallium nitride layer. These high defect densities may result from mismatches in lattice parameters between the buffer layer **102b** and the underlying gallium nitride layer **104**, and/or other causes. These high defect densities may impact the performance of microelectronic devices formed in the underlying gallium nitride layer **104**.

Still continuing with the description of Figure 6, the underlying gallium nitride layer **104** includes the plurality of sidewalls **105** that may be defined by the plurality of posts **106** and/or the plurality of trenches **107**. As was described above, the sidewalls may be oblique and of various elongated shapes. Also as was described above, the gallium nitride posts **106** are capped with a capping layer such as a mask **109**, preferably comprising silicon nitride.

Continuing with the description of Figure 6, the lateral gallium nitride layer **108a** extends laterally and vertically from the plurality of sidewalls **105** of the underlying gallium nitride layer **104**. The overgrown lateral gallium nitride **108b** extends from the lateral gallium nitride layer **108a**. The lateral gallium nitride layer **108a** and the overgrown lateral gallium nitride layer **108b** may be formed using metalorganic vapor phase epitaxy at about 1000-1100°C and about 45 Torr. Precursors of triethygallium (TEG) at about 13-39μmol/min and ammonia (NH_3) at about 1500 sccm may be used in combination with an about 3000 sccm H_2 diluent, to form the lateral gallium nitride layer **108a** and the overgrown lateral gallium nitride layer **108b**.

As shown in Figure 6, the lateral gallium nitride layer **108a** coalesces at the interfaces **108c** to form a continuous lateral gallium nitride semiconductor layer **108a** in the trenches. It has been found that the dislocation densities in the underlying gallium nitride layer **104** generally do not propagate laterally from the sidewalls **105** with the same density as vertically from the underlying gallium nitride layer **104**. Thus, the lateral gallium nitride layer **108a** can have a relatively low dislocation defect density, for example less than about 10^4 cm^{-2}. From a practical standpoint, this may be regarded as defect-free. Accordingly, the lateral gallium nitride layer **108a** may form device quality gallium nitride semiconductor material. Thus, as shown in

Figure 6, microelectronic devices **110** may be formed in the lateral gallium nitride semiconductor layer **108a**.

Still referring to Figure 6, the overgrown lateral gallium nitride layer **108b** coalesces at the interfaces **108d** to form a continuous overgrown lateral gallium nitride semiconductor layer **108b** over the masks. It has been found that the dislocation densities in the underlying gallium nitride layer **104** and of the lateral gallium nitride layer **108a** generally do not propagate laterally with the same density as vertically from the underlying gallium nitride layer **104** and the lateral gallium nitride layer **108a**. Thus, the overgrown lateral gallium nitride layer **108b** also can have a relatively low defect density, for example less than about 10^4 cm^{-2}. Accordingly, the overgrown lateral gallium nitride layer **108b** may also form device quality gallium nitride semiconductor material. Thus, as shown in Figure 6, microelectronic devices **110** may also be formed in the overgrown lateral gallium nitride semiconductor layer **108b**.

Referring now to Figures 7 and 8, other embodiments of gallium nitride semiconductor structures and fabrication methods according to the present invention will now be described. Gallium nitride structures are fabricated as was already described in connection with Figures 1-6 using different spacings or dimensions for the posts and trenches. In Figure 7, a small post-width / trench-width ratio is used to produce discrete gallium nitride structures. In Figure 8, a large post-width / trench-width ratio is used, to produce other discrete gallium nitride structures.

Referring now to Figure 7, using a small post-width / trench-width ratio, gallium nitride semiconductor structures of Figure 7 are fabricated as was already described in connection with Figures 1-4. Still referring to Figure 7, growth is allowed to continue until the overgrown lateral fronts coalesce over the mask **109** at the interfaces **108d**, to form a continuous overgrown lateral gallium nitride semiconductor layer over the mask **109**. The total growth time may be approximately 60 minutes. As shown in Figure 7, microelectronic devices **110** may be formed in the overgrown lateral gallium nitride layer **108b**.

Referring now to Figure 8, using a large post-width / trench-width ratio, gallium nitride semiconductor structures of Figure 8 are fabricated as was already described in connection with Figure 1-4. Still referring to Figure 8, growth is allowed to continue until the overgrown lateral fronts coalesce in the trenches **107** at the

interfaces **108c**, to form a continuous gallium nitride semiconductor layer **108a** in the trenches **107**. The total growth time may be approximately 60 minutes. As shown in Figure 8, microelectronic devices **110** may be formed in the pendeoepitaxial gallium nitride layer **108a**.

Additional discussion of methods and structures of the present invention will now be provided. The trenches **107** and are preferably rectangular trenches that preferably extend along the $<11\bar{2}0>$ and/or $<1\bar{1}00>$ directions on the underlying gallium nitride layer **104**. Truncated triangular stripes having $(1\bar{1}01)$ slant facets and a narrow (0001) top facet may be obtained for trenches along the $<11\bar{2}0>$ direction. Rectangular stripes having a (0001) top facet, $(11\bar{2}0)$ vertical side faces and $(1\bar{1}01)$ slant facets may be grown along the $<1\bar{1}00>$ direction. For growth times up to 3 minutes, similar morphologies may be obtained regardless of orientation. The stripes develop into different shapes if the growth is continued.

The amount of lateral growth generally exhibits a strong dependence on trench orientation. The lateral growth rate of the $<1\bar{1}00>$ oriented is generally much faster than those along $<11\bar{2}0>$. Accordingly, it is most preferred to orient the trenches so that they extend along the $<1\bar{1}00>$ direction of the underlying gallium nitride layer **104**.

The different morphological development as a function of orientation appears to be related to the stability of the crystallographic planes in the gallium nitride structure. Trenches oriented along $<11\bar{2}0>$ may have wide $(1\bar{1}00)$ slant facets and either a very narrow or no (0001) top facet depending on the growth conditions. This may be because $(1\bar{1}01)$ is the most stable plane in the gallium nitride wurtzite crystal structure, and the growth rate of this plane is lower than that of others. The $\{1\bar{1}01\}$ planes of the $<1\bar{1}00>$ oriented trenches may be wavy, which implies the existence of more than one Miller index. It appears that competitive growth of selected $\{1\bar{1}01\}$ planes occurs during the deposition which causes these planes to become unstable and which causes their growth rate to increase relative to that of the $(1\bar{1}01)$ of trenches oriented along $<11\bar{2}0>$.

The morphologies of the gallium nitride layers selectively grown from trenches oriented along $<1\bar{1}00>$ are also generally a strong function of the growth

temperatures. Layers grown at 1000°C may possess a truncated triangular shape. This morphology may gradually change to a rectangular cross-section as the growth temperature is increased. This shape change may occur as a result of the increase in the diffusion coefficient and therefore the flux of the gallium species along the (0001) top plane onto the $\{1\bar{1}01\}$ planes with an increase in growth temperature. This may result in a decrease in the growth rate of the (0001) plane and an increase in that of the $\{1\bar{1}01\}$. This phenomenon has also been observed in the selective growth of gallium arsenate on silicon dioxide. Accordingly, temperatures of 1100°C appear to be most preferred.

The morphological development of the gallium nitride regions also appears to depend on the flow rate of the TEG. An increase in the supply of TEG generally increases the growth rate in both the lateral and the vertical directions. However, the lateral/vertical growth rate ratio decrease from about 1.7 at the TEG flow rate of about 13μmol/min to 0.86 at about 39μmol/min. This increased influence on growth rate along <0001> relative to that of $<11\bar{2}0>$ with TEG flow rate may be related to the type of reactor employed, wherein the reactant gases flow vertically and perpendicular to the substrate. The considerable increase in the concentration of the gallium species on the surface may sufficiently impede their diffusion to the $\{1\bar{1}01\}$ planes such that chemisorption and gallium nitride growth occur more readily on the (0001) plane.

Continuous 2μm thick gallium nitride semiconductor layers may be obtained using 7μm wide trenches spaced 3μm apart and oriented along $<1\bar{1}00>$, at about 1100°C and a TEG flow rate of about 26μmol/min. Continuous 2μm thick gallium nitride semiconductor layers may also be obtained using 3μm wide trenches spaced 2μm apart and oriented along $<1\bar{1}00>$, also at about 1100°C and a TEG flow rate of about 26μmol/min. The continuous gallium nitride semiconductor layers may include subsurface voids that form when two growth fronts coalesce. These voids may occur most often using lateral growth conditions wherein rectangular trenches and/or mask openings having vertical $\{11\bar{2}0\}$ side facets developed.

The continuous gallium nitride semiconductor layers may have a microscopically flat and pit-free surface. The surfaces of the laterally grown gallium nitride layers may include a terrace structure having an average step height of 0.32nm. This terrace structure may be related to the laterally grown gallium nitride, because it

is generally not included in much larger area films grown only on aluminum nitride buffer layers. The average RMS roughness values may be similar to the values obtained for the underlying gallium nitride layer **104**.

Threading dislocations, originating from the interface between the underlying gallium nitride layer **104** and the buffer layer **102b**, appear to propagate to the top surface of the underlying gallium nitride layer **104**. The dislocation density within these regions is approximately 10^9 cm^{-2}. By contrast, threading dislocations do not appear to readily propagate laterally. Rather, the lateral gallium nitride layer **108a** and the overgrown lateral gallium nitride layer **108b** contain only a few dislocations. In the lateral gallium nitride layer **108a**, the few dislocations may be formed parallel to the (0001) plane via the extension of the vertical threading dislocations after a 90° bend in the regrown region. These dislocations do not appear to propagate to the top surface of the overgrown gallium nitride layer.

As described, the formation mechanism of the selectively grown gallium nitride layers is lateral epitaxy. The two main stages of this mechanism are lateral (or pendeoepitaxial) growth and lateral overgrowth. During pendeoepitaxial growth, the gallium nitride grows simultaneously both vertically and laterally. The deposited gallium nitride grows selectively on the sidewalls more rapidly than it grows on the mask **109**, apparently due to the much higher sticking coefficient, s, of the gallium atoms on the gallium nitride sidewall surface ($s=1$) compared to on the mask ($s<<1$) and substrate ($s<1$). Ga or N atoms should not readily bond to the mask and substrate surface in numbers and for a time sufficient to cause gallium nitride nuclei to form. They would either evaporate or diffuse along the mask and substrate surface to the ends of the mask or substrate and onto the sidewalls. During lateral overgrowth, the gallium nitride also grows simultaneously both vertically and laterally. Once the pendeoepitaxial growth emerges over the masks, Ga or N atoms should still not readily bond to the mask surface in numbers and for a time sufficient to cause gallium nitride nuclei to form. They would still either evaporate or diffuse along the mask to the ends of the mask and onto the pendeoepitaxial gallium nitride vertical surfaces.

Surface diffusion of gallium and nitrogen on the gallium nitride may play a role in gallium nitride selective growth. The major source of material appears to be derived from the gas phase. This may be demonstrated by the fact that an increase in

the TEG flow rate causes the growth rate of the (0001) top facets to develop faster than the $(1\bar{1}01)$ side facets and thus controls the lateral growth.

In conclusion, pendeoepitaxial and lateral epitaxial overgrowth may be obtained from sidewalls of an underlying masked gallium nitride layer via MOVPE. The growth may depend strongly on the sidewall orientation, growth temperature and TEG flow rate. Coalescence of pendeoepitaxial grown and lateral overgrown gallium nitride regions to form regions with both extremely low densities of dislocations and smooth and pit-free surfaces may be achieved through 3μm wide trenches between 2μm wide posts and extending along the $<1\bar{1}00>$ direction, at about 1100°C and a TEG flow rate of about 26μmol/min. The pendeoepitaxial and lateral overgrowth of gallium nitride from sidewalls via MOVPE may be used to obtain low defect density regions for microelectronic devices over the entire surface of the thin film.

In the drawings and specification, there have been disclosed typical preferred embodiments of the invention and, although specific terms are employed, they are used in a generic and descriptive sense only and not for purposes of limitation, the scope of the invention being set forth in the following claims.

That Which is Claimed Is:

1. A method of fabricating a gallium nitride semiconductor layer comprising the steps of:

masking an underlying gallium nitride layer on a silicon carbide substrate with a mask that includes an array of openings therein;

etching the underlying gallium nitride layer through the array of openings to define a plurality of posts in the underlying gallium nitride layer and a plurality of trenches therebetween, the posts each including a sidewall and a top having the mask thereon; and

laterally growing the sidewalls of the posts into the trenches to thereby form a gallium nitride semiconductor layer.

2. A method according to Claim 1 wherein the step of laterally growing comprises the step of laterally growing the sidewalls of the posts into the trenches until the laterally grown sidewalls coalesce in the trenches to thereby form a gallium nitride semiconductor layer.

3. A method according to Claim 1 wherein the step of laterally growing comprises the step of laterally overgrowing the laterally grown sidewalls of the posts in the trenches onto the mask on the tops of the posts, to thereby form a gallium nitride semiconductor layer.

4. A method according to Claim 3 wherein the step of laterally growing comprises the step of laterally overgrowing the laterally grown sidewalls of the posts in the trenches onto the mask on the tops of the posts until the laterally grown sidewalls coalesce on the mask, to thereby form a gallium nitride semiconductor layer.

5. A method according to Claim 1 wherein the laterally growing step is followed by the step of forming microelectronic devices in the gallium nitride semiconductor layer.

6. A method according to Claim 1 wherein the laterally growing step comprises the step of laterally growing the sidewalls of the posts into the trenches using metalorganic vapor phase epitaxy.

7. A method according to Claim 1 wherein the masking step comprises the step of masking an underlying gallium nitride layer on a buffer layer on a silicon carbide substrate with a mask that includes an array of openings therein.

8. A method according to Claim 1 wherein the etching step comprises the step of etching the underlying gallium nitride layer and the silicon carbide substrate through the array of openings to define a plurality of posts in the underlying gallium nitride layer and a plurality of trenches therebetween, the posts each including a sidewall and a top having the mask thereon, the trenches including trench floors in the silicon carbide substrate.

9. A method according to Claim 7 wherein the etching step comprises the step of etching the underlying gallium nitride layer, the buffer layer and the silicon carbide substrate through the array of openings to define a plurality of posts in the underlying gallium nitride layer and a plurality of trenches therebetween, the posts each including a sidewall and a top having the mask thereon, the trenches including trench floors in the silicon carbide substrate.

10. A method according to Claim 1 wherein the masking step comprises the step of masking the underlying gallium nitride layer on a silicon carbide substrate with a mask that includes an array of stripe openings therein, the stripe openings extending along a <1100> direction of the underlying gallium nitride layer.

11. A method according to Claim 1 wherein the underlying gallium nitride layer includes a defect density, and wherein the laterally growing step comprises the step of laterally growing the sidewalls of the posts into the trenches to thereby form a gallium nitride semiconductor layer of lower defect density than the defect density.

12. A method according to Claim 1 wherein the masking step is preceded by the step of forming an underlying gallium nitride layer on a silicon carbide substrate.

13. A method according to Claim 7 wherein the masking step is preceded by the steps of:

forming a buffer layer on a silicon carbide substrate; and

forming an underlying gallium nitride layer on a buffer layer, opposite the silicon carbide substrate.

14. A method of fabricating a gallium nitride semiconductor layer comprising the steps of:

providing a silicon carbide substrate, a gallium nitride layer on the silicon carbide substrate and a capping layer on the gallium nitride layer opposite the silicon carbide substrate, the gallium nitride layer including a plurality of posts and a plurality of trenches therebetween, the trenches defining a plurality of openings in the capping layer;

laterally and vertically growing sidewalls of the posts into the trenches and through the openings in the capping layer to thereby form a lateral gallium nitride layer in the trenches that extends vertically through the openings in the capping layer; and

laterally overgrowing the lateral gallium nitride layer that extends through the openings in the capping layer onto the capping layer to thereby form an overgrown lateral gallium nitride layer.

15. A method according to Claim 14 wherein the steps of laterally and vertically growing the sidewalls and laterally overgrowing the lateral gallium nitride layer are performed without vertically growing gallium nitride on the capping layer.

16. A method according to Claim 14 wherein the step of laterally overgrowing the lateral gallium nitride layer comprises the step of laterally overgrowing the lateral gallium nitride layer that extends through the openings in the capping layer onto the capping layer until the overgrown lateral gallium nitride layer

coalesces on the capping layer to thereby form a continuous overgrown lateral gallium nitride layer.

17. A method according to Claim 14 wherein the step of laterally overgrowing the lateral gallium nitride layer is followed by the step of forming microelectronic devices in the overgrown lateral gallium nitride layer.

18. A method according to Claim 14 wherein the providing step comprises the steps of:

masking an underlying gallium nitride layer on a silicon carbide substrate with a mask that includes an array of openings therein;

etching the underlying gallium nitride layer through the array of openings to define a plurality of posts in the gallium nitride layer and a plurality of trenches therebetween, the posts each including a sidewall and a top having the mask thereon to provide the capping layer.

19. A method according to Claim 18 wherein the masking step comprises the step of masking an underlying gallium nitride layer on a buffer layer on a silicon carbide substrate with a mask that includes an array of openings therein.

20. A method according to Claim 18 wherein the etching step comprises the step of etching the underlying gallium nitride layer and the silicon carbide substrate through the array of openings to define a plurality of posts in the underlying gallium nitride layer and a plurality of trenches therebetween, the posts each including a sidewall and a top having the mask thereon, the trenches including trench floors in the silicon carbide substrate.

21. A method according to Claim 19 wherein the etching step comprises the step of etching the underlying gallium nitride layer, the buffer layer and the silicon carbide substrate through the array of openings to define a plurality of posts in the underlying gallium nitride layer and a plurality of trenches therebetween, the posts each including a sidewall and a top having the mask thereon, the trenches including trench floors in the silicon carbide substrate.

22. A method according to Claim 14 wherein the underlying gallium nitride layer includes a defect density, and wherein the laterally and vertically growing step comprises the step of laterally and vertically growing the sidewalls of the posts into the trenches and through the openings in the capping layer to thereby form a lateral gallium nitride semiconductor layer of lower defect density than the defect density.

23. A gallium nitride semiconductor structure, comprising:

a silicon carbide substrate;

a plurality of gallium nitride posts on the silicon carbide substrate, the posts each including a sidewall and a top, and defining a plurality of trenches therebetween;

a capping layer on the tops of the posts; and

a lateral gallium nitride layer that extends laterally from the sidewalls of the posts into the trenches.

24. A structure according to Claim 23 wherein the lateral gallium nitride layer is a continuous lateral gallium nitride layer that extends between adjacent sidewalls across the trenches therebetween.

25. A structure according to Claim 23 wherein the lateral gallium nitride layer also extends vertically in the trenches, to beyond the capping layer.

26. A structure according to Claim 25 further comprising:

an overgrown lateral gallium nitride layer that extends laterally from the lateral gallium nitride layer onto the capping layer.

27. A structure according to Claim 26 wherein the overgrown lateral gallium nitride layer is a continuous overgrown lateral gallium nitride layer that extends between adjacent sidewalls across the capping layer therebetween.

28. A structure according to Claim 23 further comprising a plurality of microelectronic devices in the lateral gallium nitride layer.

29. A structure according to Claim 25 further comprising a plurality of microelectronic devices in the lateral gallium nitride layer that extends vertically in the trenches, beyond the capping layer.

30. A structure according to Claim 26 further comprising a plurality of microelectronic devices in the overgrown lateral gallium nitride layer.

31. A structure according to Claim 23 further comprising a buffer layer between the silicon carbide substrate and the plurality of posts.

32. A structure according to Claim 23 wherein the trenches extend into the silicon carbide substrate.

33. A structure according to Claim 31 wherein the trenches extend through the buffer layer and into the silicon carbide substrate.

34. A structure according to Claim 23 wherein the posts are of a defect density and wherein the lateral gallium nitride layer is of lower defect density than the defect density.

35. A structure according to Claim 26 wherein the posts are of a defect density and wherein the overgrown lateral gallium nitride layer is of lower defect density than the defect density.

FIG. 1

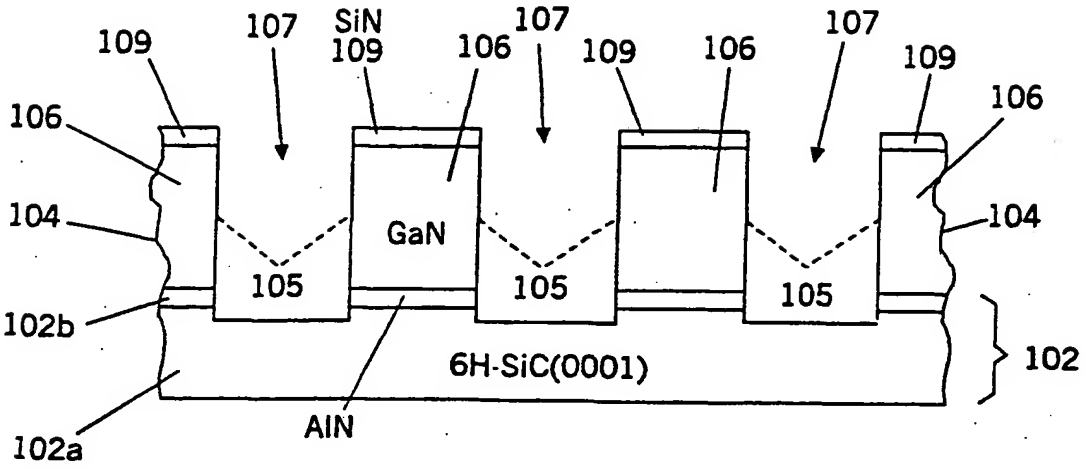
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FIG. 2

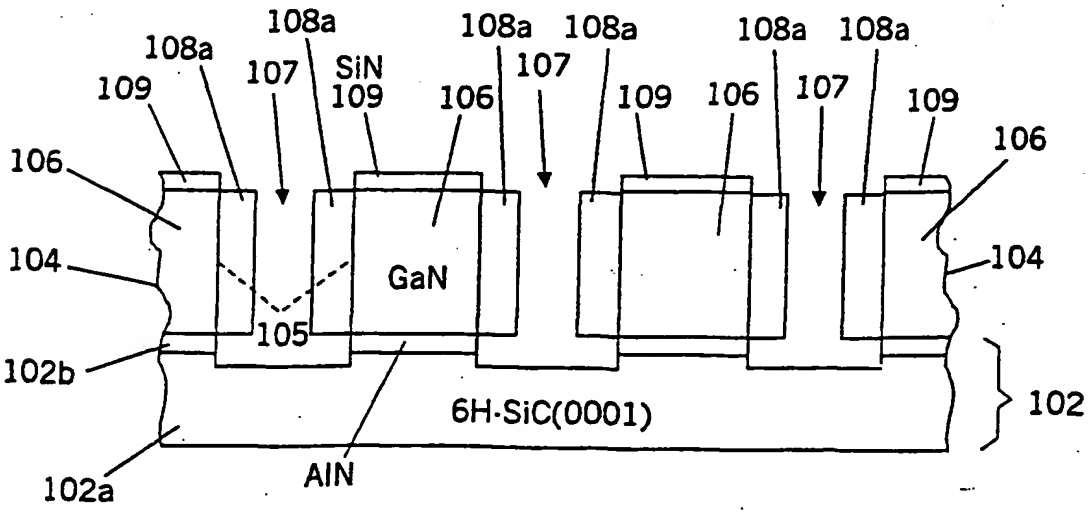
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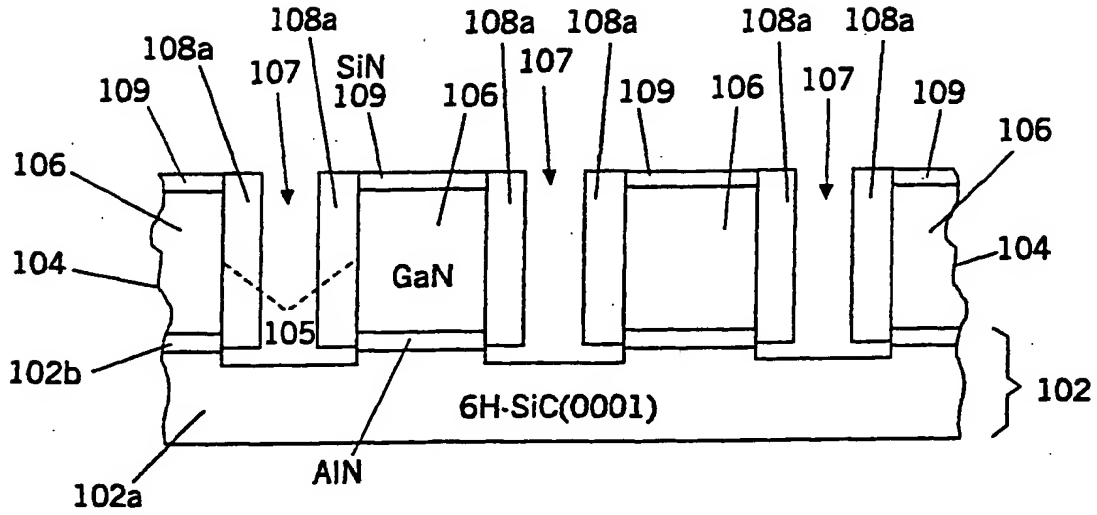
FIG. 3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AlN
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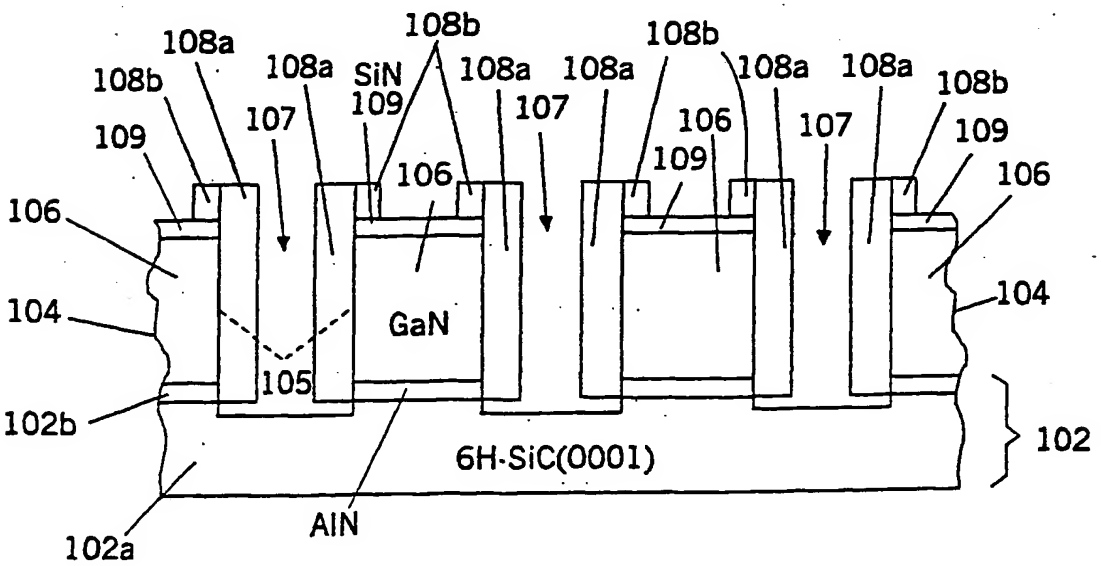
FIG. 4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AlN
102a

FIG. 5

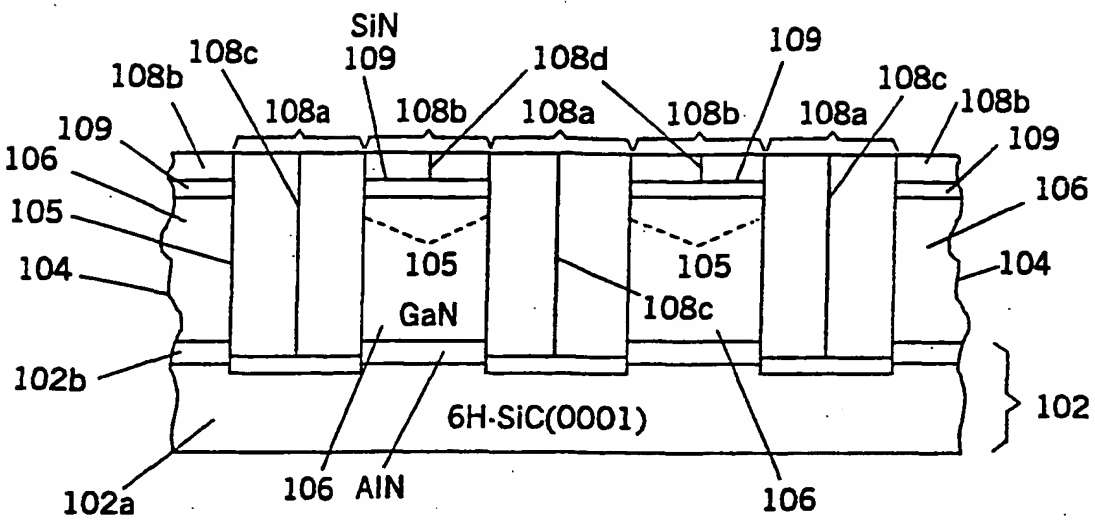
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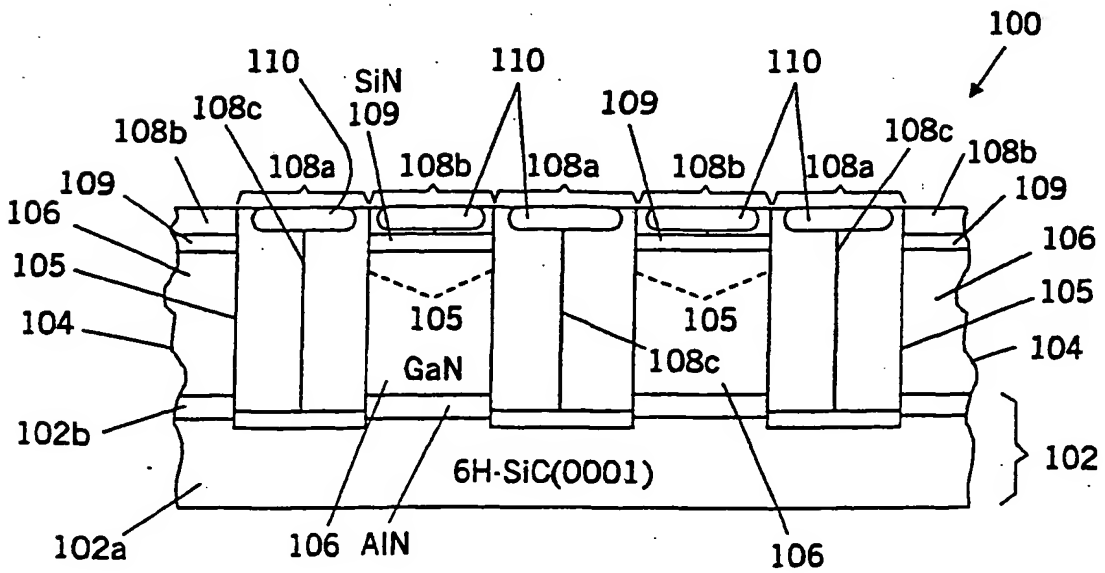
FIG. 6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102a
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AlN
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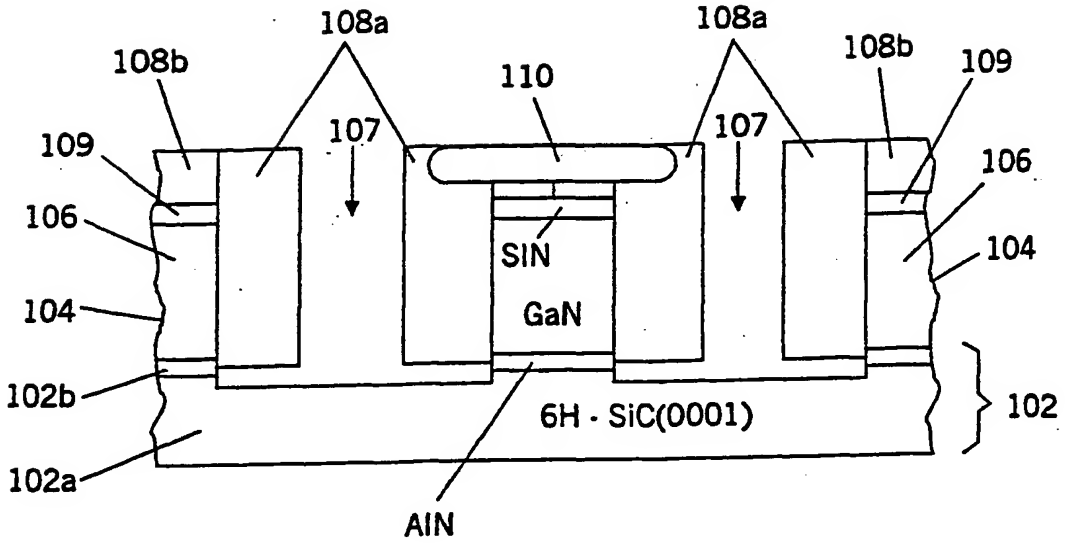
FIG. 7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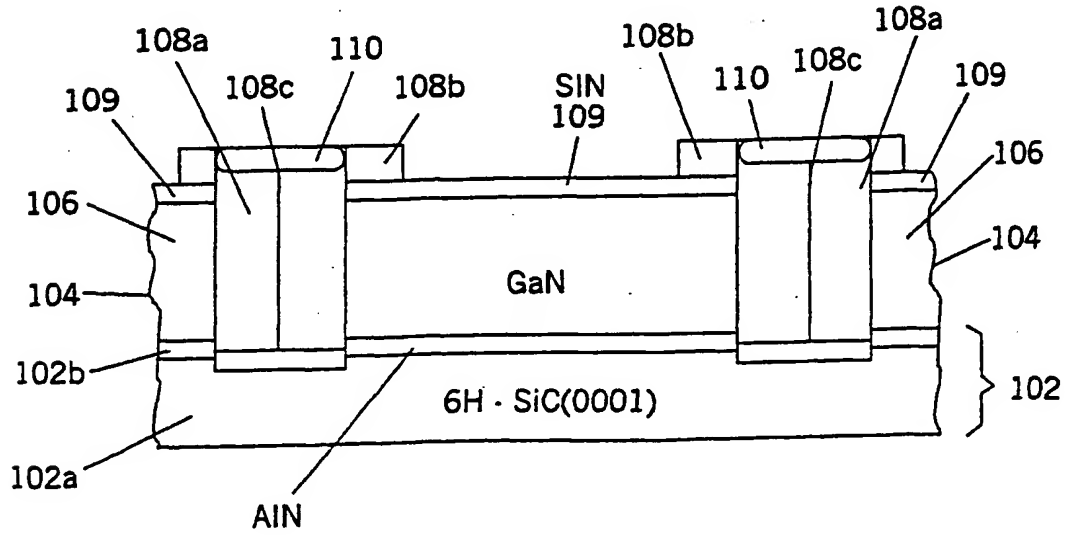
102a
AlN

FIG. 8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102a
AlN

INTERNATIONAL SEARCH REPORT

Inter onal Application No
PCT/US 99/28056

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L21/20

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L C30B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 98 47170 A (NICHIA CHEMICAL INDUSTRIES LTD (JP); KIYOKU HIROYUKI (JP) ET AL) 22 October 1998 (1998-10-22) -& EP 0 942 459 A (NICHIA CHEMICAL INDUSTRIES LTD) 15 September 1999 (1999-09-15) paragraph '0032! paragraph '0063! - paragraph '0083! example 35 figure 7	1-9, 11-35

-/—

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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"O" document referring to an oral disclosure, use, exhibition or other means

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Date of the actual completion of the international search	Date of mailing of the international search report
13 April 2000	26/04/2000

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Tx. 31 651 epo nl, Fax: (+31–70) 340–3016	Köpf, C

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INTERNATIONAL SEARCH REPORT

Inter. ...nal Application No
PCT/US 99/28056

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
A	NAM O-H ET AL: "Lateral epitaxy of low defect density GaN layers via organometallic vapor phase epitaxy" APPLIED PHYSICS LETTERS, USA, vol. 71, no. 18, 3 November 1997 (1997-11-03), pages 2638-2640, XP000726169 ISSN: 0003-6951 the whole document	1,6,7, 10-14,23
P,X	EP 0 951 055 A (HEWLETT PACKARD CO) 20 October 1999 (1999-10-20) paragraph '0030! - paragraph '0036! paragraph '0046! - paragraph '0048!; figure 3	1-5,8, 11,12, 14,16, 17, 22-28, 34,35
P,X	LINTHICUM K J ET AL: "Process routes for low defect-density GaN on various substrates employing pendeo-epitaxial growth techniques" MRS INTERNET JOURNAL OF NITRIDE SEMICONDUCTOR RESEARCH, 1999, vol. 4S1, no. 4.9, 30 November 1998 (1998-11-30) - 4 December 1999 (1999-12-04), XP002117210 Fall Meeting of the Materials Reserach Society, Boston ISSN: 1092-5783 the whole document	1-4, 6-16, 18-27, 31-35

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/US 99/28056

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
WO 9847170 A	22-10-1998	CA 2258080 A	22-10-1998
		EP 0942459 A	15-09-1999
		JP 11191657 A	13-07-1999
		JP 11191637 A	13-07-1999
		JP 11191659 A	13-07-1999
		JP 11219910 A	10-08-1999
EP 0951055 A	20-10-1999	JP 2000021771 A	21-01-2000

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23 November 1999 (23.11.1999)

(25) Filing Language: English

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(71) Applicant *(for all designated States except US)*: NORTH CAROLINA STATE UNIVERSITY [US/US]; 1 Holladay Hall, Campus Box 7003, Raleigh, NC 27695-7003 (US).

(72) Inventors; and
(75) Inventors/Applicants *(for US only)*: LINTHICUM, Kevin, J. [US/US]; 474 Crosslink Drive, Angier, NC 27501 (US). GEHRKE, Thomas [DE/US]; 116B Bim Street, Carrboro, NC 27510 (US). THOMSON, Darren, B. [US/US]; 425 W. Cornwall Road, Cary, NC 27511 (US). CARLSON, Eric, P. [US/US]; 1208 Southern Oaks Drive, Raleigh, NC 27603 (US). RAJAGOPAL, Pradeep [IN/US]; Apartment 102, 2502 Avent Ferry Road, Raleigh, NC 27606 (US). DAVIS, Robert, F. [US/US]; 5705 Calton Drive, Raleigh, NC 27612 (US).

(74) Agents: BIGEL, Mitchell, S. et al.; Myers, Bigel, Sibley, & Sajovec, P.A., P.O. Box 37428, Raleigh, NC 27627 (US).

(81) Designated States *(national)*: AE, AL, AM, AT, AT (utility model), AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, CZ (utility model), DE, DE (utility model), DK, DK (utility model), EE, EE (utility model), ES, FI, FI (utility model), GB, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SK (utility model), SL, TJ, TM, TR, TT, UA, UG, US, UZ, VN, YU, ZA, ZW.

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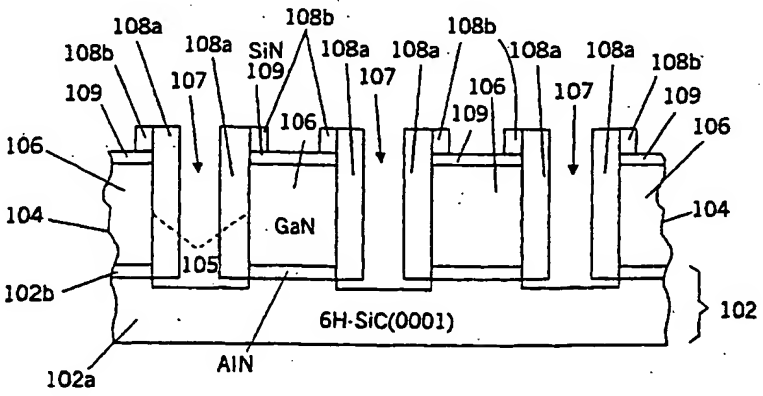
(54) Title: FABRICATION OF GALLIUM NITRIDE LAYERS BY LATERAL GROWTH



(57) Abstract: An underlying gallium nitride layer (104) on a silicon carbide substrate (102) patterned with a mask (109) that includes an array of openings therein, and is etched through the array of openings to define posts (106) in the underlying gallium nitride layer and trenches (107) therebetween. The posts each include a sidewall (105) and a top having the mask thereon. The sidewalls of the posts are laterally grown into the trenches to thereby form a gallium nitride semiconductor layer (108a). During this lateral growth, the mask prevents nucleation and vertical growth from the tops of the posts. Accordingly, growth proceeds laterally into the trenches, suspended from the sidewalls of the posts. The sidewalls of the posts may be laterally grown into the trenches until the laterally grown sidewalls coalesce in the trenches to thereby form a gallium nitride semiconductor layer. The lateral growth from the sidewalls of the posts may be continued so that the gallium nitride layer grows vertically through the openings in the mask and laterally overgrows onto the mask on the tops of the posts, to thereby form a gallium nitride semiconductor layer (108b). The lateral overgrowth can be continued until the grown sidewalls coalesce on the mask to thereby form a continuous gallium nitride semiconductor layer. Microelectronic devices (110) may be formed in the continuous gallium nitride semiconductor layer.

WO 00/33365 A1

WO 00/33365 A1

(84) **Designated States** *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

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For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.